Porous Silicon on Insulator Technology

Abstract:

In this research, the structure, optical, and electrical properties of porous silicon prepared by electrochemical etching at current density 50 mA /cm^2 with etching time 10 min, before and after rapid thermal oxidation process (RTO) at different oxidation temperature from (500-700) Ċ and constant oxidation time 60 s. Under optimum conditions, the pore size decreased after RTO leads to decrease porosity, the refractive index decreased for porous silicon (PS) and increased after oxidation. Electrical properties was showed an increase in rectification ratio after oxidation, where it varied from (3.93 to 158.8), the ideality factor which describes an approach the device from ideality characteristics founded decrease with increasing oxidation temperature where it varied from (9 to 5.4), the barrier height increased from (0.561 to 0.698 eV). The oxidation process improves electrical conductivity for electronic device by decreasing saturation current density that initiated from minority carriers, where (OPS/PS/Si) work as anti-reflected coating that benefit to eliminate swings effect and standing waves in photoresist .

Key words: Oxidize Porous Silicon, Structure - Optical properties, Electrical properties, Rectification ratio, RTO .

1.Introduction:

Porous silicon is different from bulk silicon, after silicon surface is etched by the current in an electrolytic solution and become porous, the energy band is folded and its indirect energy gap becomes a direct band gap, so the electro-optics conversion efficiency increased, therefore the quantum coefficient of photon is increased[1]. Uhlir in 1956 founded PS when he performs the electrochemical etching of silicon. Canham in 1990, displayed that certain PS materials have great efficiency of photoluminescence (PL) at room temperature in the visible: a surprising result, since the PL efficiency of bulk silicon (Si) is low because of the indirect energy band gap and tiny non-radioactive life time because of the partial dissolution of silicon, causes: i) the formation of small silicon nano crystals in the PS material; ii) the reduction of the effective refractive index of PS with respect to silicon, and hence an increased light extraction efficiency from PS; and iii) the spatial confinement of the excited carriers in small silicon regions where non-radiative recombination center is mostly absent. In general, PS is an interconnected network of air holes (pores) in Si. PS classified according to the pore diameter, which can vary from a few nanometers to a few microns depending on the formation parameters[2].

As porous silicon is grown in the electrical devices takes some disadvantages: Optical and electrical features are not unchanging, photo sensitivity and photo current are not high sufficient, dark current is not lower sufficient, which confines the action of the device[3]. With stable physical and optical features of as-anodized porous silicon, several techniques have been developed the most effective methods is the oxidation by formation of SiO_2 layer on PS cores[4]. Various oxidation approaches, such as chemical oxidation , anodic oxidation[5], conventional furnace oxidation [6], thermal oxidation [7,8] and aging oxidation [9], are used to generate a more stable O-passivated surface to replace the unstable H-passivated surface. Furthermore, those oxidation ways can improve efficiency of light emission[10,11]. The scientists and researchers observed that, the film, which growth by anodic oxidation method stay several chemical ions after the deposition that has an effect on electrical properties, which cause instability of the device after oxidation with having different stress. The same process occurs with using deposition techniques by chemical vapor or plasma interaction. In addition, Oxidation by plasma may etch material surface rather than oxidized it. Using thermal oxidation the best silicon /PS interface can be made-up[4]. There are three types of thermal oxidation: Adiabatic, thermal flux oxidation and rapid thermal oxidation. The main difference between these types is heat energy and time, which provide

heat to the material compared with thermal response time (t_{th}) which defines as equation 1.[12].Then the incident energy is absorbed in the surface region the heat treatment classified as adiabatic oxidation. The most important example of adiabatic oxidation is the oxidation which occur at room temperature in ambient (ageing) [11]. While thermal flux oxidation occurs when thermal response time is like heat treatment time, the incident thermal energy can diffuse into the bulk of the sample and non steady –state temperature gradients are present , the rapid thermal oxidation occurs if thermal oxidation time is much shorter than duration of heat treatment then there is enough time for the temperature distribution to reach a steady state value ,have constant temperature gradient (steady state oxidation).The magnitude of these constant temperature gradients ΔT can be calculated from the well-known relation 2.[12]:

$$t_{th}=\frac{D_{th}^2}{N_{th}} \quad \ldots(1)$$

$$\Delta T=\frac{\Delta H}{k_{th}} \quad \ldots(2)$$

Where D_{th} (cm) is the penetration depth, N_{th} (cm^2/s) is the diffusivity. Adiabatic thermal oxidation occurs when thermal response time is longer than heat treatment time, ΔH is the energy flux in W, k_{th} in W $m^{-1}K^{-1}$ is thermal conductivity at the oxidation temperature. In a carefully deigned heating system (such as diffusion furnace with illumination by quartz-halogen lamps. The temperature gradient is negligible and constant temperature zero temperature gradient rather than other types.

The aim of the research to fabricate planar porous Silicon metal-semiconductor-metal photo detector, and applied rapid thermal oxidation (RTO) method to improve the photo current and photo sensitivity of porous silicon metal-semiconductor-metal photo detector to improve dark current of the present invention so that the application of planar metal-semiconductor-metal photo detector in an optoelectronic integrated circuit is even more widespread.

2. Experimental:

In this work, the porous silicon is prepared from single crystalline p-type silicon (100) oriented (7-10 Ω.cm) with thickness 508 μm as starting substrates. The substrates were cutting into rectangles with ($1\times1.5cm^2$) area. A mixture of HF and Ethanol (1:4) to obtain 10% HF concentration cleans the native oxide. Electrochemical etching then performed in HF 47% concentration and Ethanol (1:1) at room temperature the electrical circuit completed after putting a Platinum electrode in a parallel way to achieve the homogenous PS layers. Current density of about (50 mA/cm^2) applied for etching time (10 min), (Figure.1) Shows the schematic diagram of electrochemical etching system. The porous area was 2 cm^2, as-prepared porous silicon was dried by rapid hot air (using sashwar) and stored in container contain ethanol to reduce oxidization and contaminations.

The rapid thermal oxidation (RTO) system is consisted from the following :(1) a tungsten halogen photo optic lamp type (OSRAM 64575) with power 1000 W based on a ceramic base. A parabolic reflector like half circuit was put under the lamp to increase the heating efficiency ,(2)A quartz tube have 2 cm diameter opening from two sides to circulate the dry oxygen source. The quartz tube attached with halogen lamp to obtain the most wanted temperature. The various RTO temperatures ranged (500-700) K at oxidation time 60 s can be measured by calibration using a thermocouple with a digital reader, which has been located above the sample.

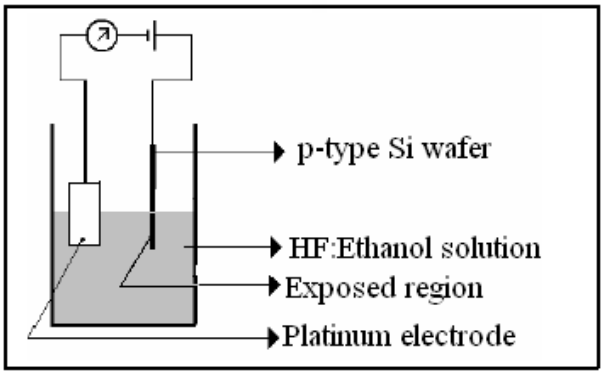

Figure1.Schematic diagram depicts the electrochemical etching system.

3. Result and discussions:

Figure 2. shows the morphology images using (SEM) of PS prepared by electrochemical etching, pore size was directly measured from SEM. It could be seen that the pore network (in black) separated by silicon crystallites (in white).For sample (a), pore size varied from (1.244 to 329.66 nm), while for sample (b) the pore size was varied from (0.837 to 221.77 nm), this significance decreased pore size after oxidation due to progress oxide inter pore , the varation in pore size attributed to entire surface shows sponge like structure.These observations confirm the presence of nanocrystalline silicon particles around the pores.By comparing Figure2 a and b, after oxidation, the pore shape is conserved in spite of size reduction. Moreover, the wall size that separate pores can be evaluated from these micrographs. That increase due to the volume expansion of silicon transformed into oxidized silicon. However, the pores did not collapse because of the initial porosity which it more important than volume expansion and the structure was allows open on the surface. Therefore, the density was nearly the same before and after oxidation about (8.79×10^{10} pore /cm^2) .The porous layer thickness measured by employing high resolution optical microscope (OLUPUS BH2) type with resolution down to 600X ,the optical microscopy connected with computer and digital camera, the porous layer thickness was (10-18 µm) this difference in thickness due to some of pore etched greater than others, we take the average of these value ,the porous layer thickness was 14 µm.

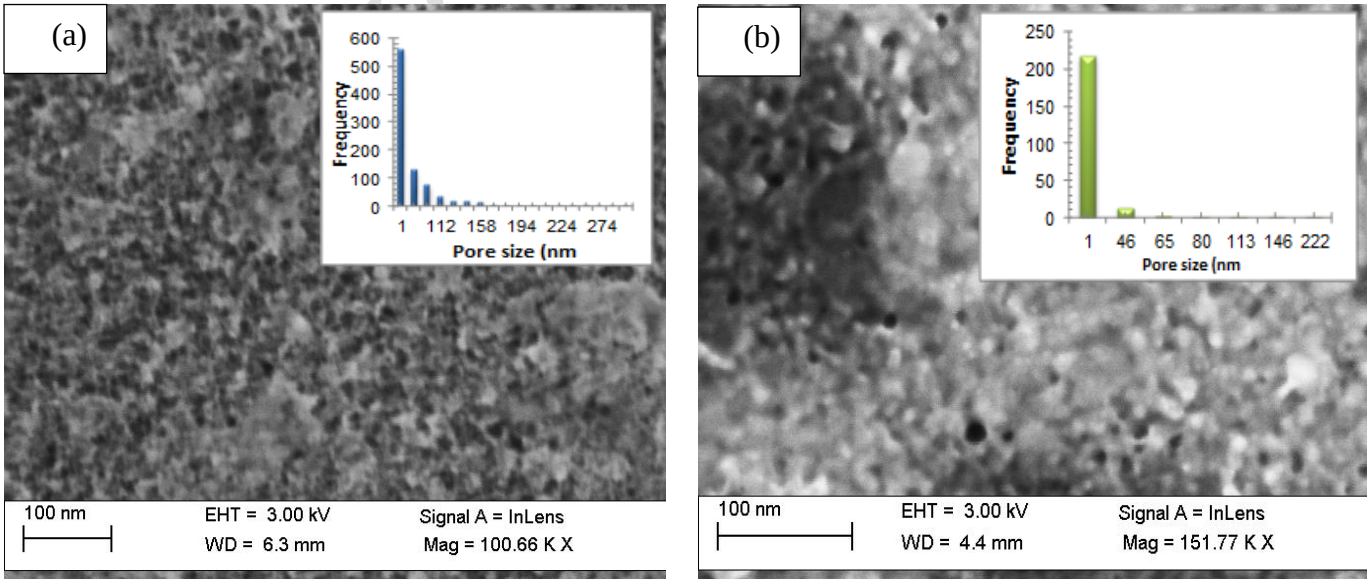

Figure 2. FESEM at current density 50 mA/cm^2 and etching time 10 min ,(a) before oxidation (b) at oxidation temperature 700 ℃ and 60 s

The porosity refers to the fraction of void within PS layer, it is with thickness the most important parameters which characterize porous silicon . The porosity of the porous silicon samples depends upon the fabrication parameters. The porosity can determin easily by weighing measurements or the geometric method using SEM analysis and is given by[10] :

$$P=\left(\frac{\pi}{2}\times 1.732\right)\left[\frac{1}{1+\frac{m}{d}}\right] \quad \ldots(3)$$

Where d is the average pore size and m is the distance between pores. Using equation (3), the porosity of the etched samples prepared has been estimated at 41 % and 25% for as prepared and after oxidation respectively.

The porosity value of the as prepared sample is higher than after oxidation . The decrease in porosity value of the samples after oxidation due to growth of oxide inter pore.

The refractive index of a porous silicon layer is dependent upon the porosity of that particular layer. Here, effective medium approximations (EMA) are used to determine the refractive index of the PS layers. The porous silicon is a composite material with a combination of single crystal silicon (c-Si) and voids and the refractive index of a porous silicon layer is expected to be lower than that of bulk silicon. The Bruggeman (equation 4)[10,11] is used to determine the refractive index (n) of porous silicon as follows:

$$P\frac{n^2_{air}-n^2_{PS}}{n^2_{air}+2n^2_{PS}}+(1-P)\frac{n^2_{Si}-n^2_{PS}}{n^2_{Si}+2n^2_{PS}}=0 \quad \ldots(4)$$

This model depends on the porosity and the morphology of the porous silicon so the refractive index as a function of porosity.

$$n_{ps}=0.5\times\left[3P(1-n^2_{si})+(2n^2_{si}-1)+\left((3P(1-n^2_{si})+(2n^2_{si}-1)\right)^2+8n^2_{si}\right)^{0.5}\right]^{0.5} \quad \ldots(5)$$

Where n_{ps}, n_{Si}, and n_{air} are the refractive indices of porous silicon, silicon and air; P is the porosity. The calculated refractive index values are given in Table 1. As the porosity increases the refractive index decreases. So the porosity is modifiable, which in turn makes refractive index also modifiable because of the control capability of its refractive index, the application of PS as an antireflection coating is very important.

From Table 1, we see that the refractive index decreases with increasing porosity attributed to the variation of the packing density. The relation between refractive index n and packing is illustrated by [13]:

$$n_{PS}=\rho n_{PS}+(1-\rho)n_{air} \quad \ldots(6)$$

Where n_{pS} and n_{air} are the refractive index of the solid part of the film and the voids, respectively. The packing density decreases with the increase of porosity. Therefore, we know that the refractive index of PS layer decreases as packing density decreases or porosity increases, which has good agreement with others[14].

Table 1. The porosity, refractive index, and packing density values of porous Si before and after RTO.

Sample preparation condition	Porosity (%)	Refractive index (n)	Packing density%
Si	**0**	3.42	34(Callister. 2006)
Before oxidation	41	2.89	78
After oxidation	25	3.1	86.77

The D.C measurements were made in the dark for a number of PS/Si and PS/ OPS/ Si samples **.** Figure 3. Shows the J-V characteristics of PS before and after the RTO, the forward current of porous is increased after oxidation this indicates improvement in the charge transfer and electrode after the RTO process .

Generally the forward current shows the presence of two distinguish regions. First, at low voltage (V_F<3kT/q), the recombination current is dominant, because the concentration of charge carriers is greater than the concentration of charge intrinsic (n p > ni^2). Therefore, for equilibrium case, recombination process will take place. This means that each excitation electron from the valence band to conduction band will recombine with a hole in the valence band. Second, at high voltage (V_F > 3KT/q), the forward current increases exponentially because the bias voltage potential exceeds the potential barrier. This potentially gives the electrons enough energy to overcome the barrier height flow and that is what called diffusion current[15,16]. In the reverse bias, there are two regions; one at low voltage, where the current increases with the applied voltage and the generating current is dominant. In the second region, the current is dependent on voltage and the diffusion current is dominant. In addition, one can notice that the forward current decreases with the increasing of etching time. When etching time increases the porous layer and the porosity increase, so that the pore walls act as carriers trapped and caused high resistivity lead to the current will be decreased [16]

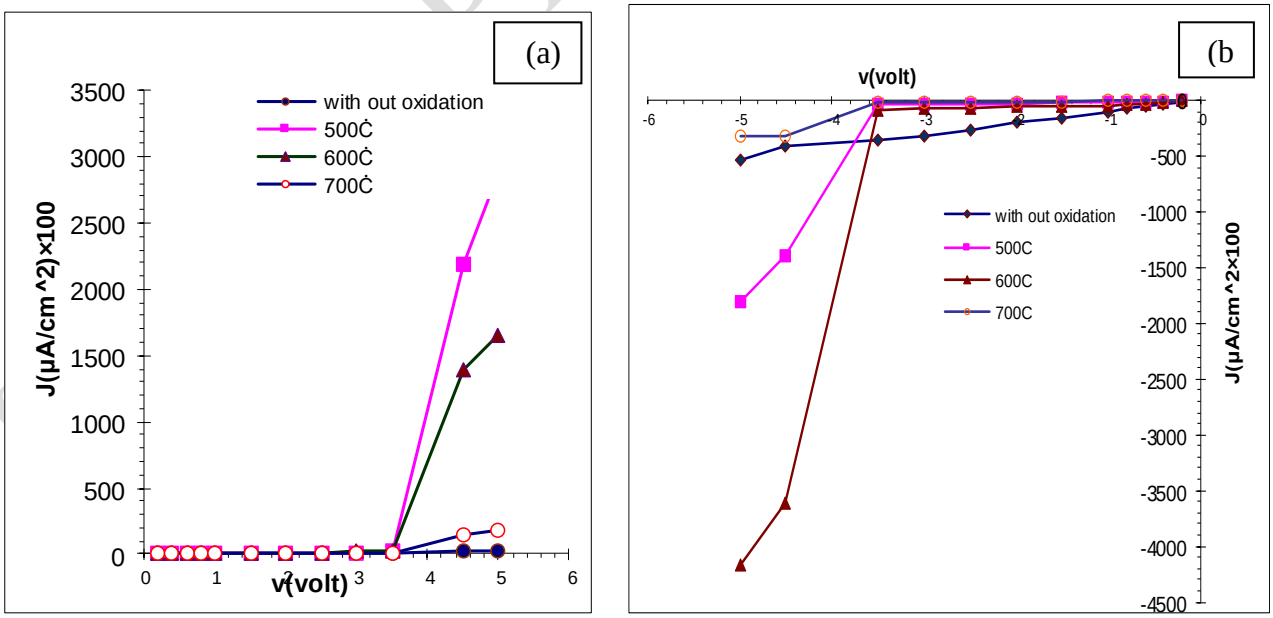

Figure 3. The J-V characteristics of Al/PS/P-Si/Al sandwich structure before and after RTO treatment at different oxidation temperatures ,(a)forword current,(b)reverse current.

Figure 4 shows the rectification ratio of PS before and after the RTO process, the rectification ratio defined as the ratio between the forward current in the reverse current [16,17], increased rectification ratio due to the formation of an Isotype hetro junction; since PS is reported to be a p-type when it is fabricated from p-type substrate and n-type when it is fabricated from n-type substrate[1,8]. It is found that at 5 volts is (3.93) for sample (a), after oxidation the rectification ratio is increased and reached (158.8) at oxidation temperature 500Ċ, this increased in rectification factor attributed to the formation of a thin oxide layer between Al metal and Si. This interface layer introduces MIS structure, which in turn leads to a decrease reverse saturation current and hence increases the rectification factor [16], other reasons for attributing increasing rectification ratio after oxidation for fresh PS the reverse current of the M/PS/Si/M structures become sensitive to the ambient due to large pore size. The increase of reverse current was observed due to increase relative humidity (R_{H2O}) [4], the RTO process caused to replace unstable hydrogen and oxygen atoms of pure oxygen that are decreasing the dangling bond that work as recombination center and decrease saturation current at that time decreasing reverse current [16]. For higher applied voltage the rectification ratio was decreased due to the avalanche effect in the local region will occur because of the wire size of the PS is very narrow, and it is incomplete depletion[18].

At a high oxidation temperature, we can observe the rectification ratio was decreased. That decreased in rectification ratio in this case due to the interface layer will be thicker and reduces the majority-carrier thermo emission current without affecting the minority carrier current .This will reduce forward current subsequently decreasing the rectification ratio[19].

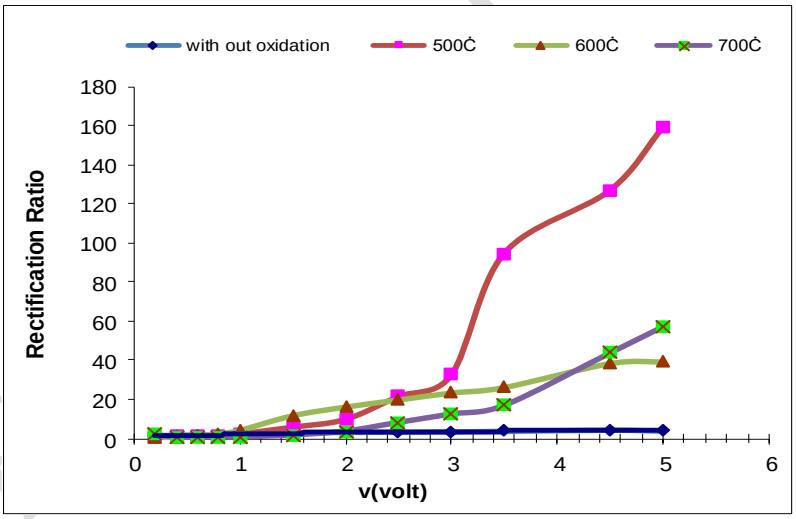

Figure 4. Shows the rectification ratio with different oxidation temperatures.

For ideal p-n junction diode. The J-V, characteristics described by Shokely equation[14]:

$$J = J_s\left[\exp\left(qV/kT\right) - 1\right] \quad \ldots(7)$$

Where J (mA/cm^2) is the current density, where J_s (mA/cm^2) is the saturation current density obtained by extrapolating the current density from the log-linear plot to V= 0, T (K) is the absolute temperature, k (J/K) is the Boltzmann's constant, q (C) is the electronic charge, V (V) is the applied voltage.

For an ideal Shottky barrier, the J-V characteristics described by an equation which is identical to the Shockley equation because of the depletion layer of a metal –semiconductor contact is similar to that on the one side abrupt (e.g., p^+-n) junction[16,17].

The diode can also exhibit bulk and on surface generation –recombination current and drift currents at high minority carrier injection levels. To correct for this additional currents, a non-ideality factor, n, is included in the Shockley equation where, the total current density, which consists of both thermo emission and tunneling, can be conveniently expressed as[12]:

$$J = J_s\left[\exp\left(qV/nKT\right) - 1\right] \quad \ldots(8)$$

Where n is the ideality factor. Equation (7) called the diode equation.

Tunneling current may become more significant. In the extreme of an ohmic contact, which is a metal contact for degenerate semiconductor , after oxidation saturation current density will be decreased due to the oxide layer to prevent tunneling of minority carrier from semiconductor to metals [1].

The ideality factor (n) describes approach the device to ideality characteristics, it derived from equation (7) and given by [12]:

$$n = \frac{q}{KT}\frac{\partial V}{\partial(\ln J)} \quad \ldots(9)$$

A semi-logarithmic relationship of forward current versus bias voltage is plotted as shown in Figure 5. The decrease in ideality factor of PS after the RTO process is observed because of the fresh sample has height ideality factor about 9 due to it has great density of state because of dangling bonds[18]. After oxidation treatment the value of ideality factor will be decreased it is varied from (9 to 5.4 at oxidation temperature 600Ċ).Figure5 shows that decreasing of ideality factor with oxidation temperature attributed to different reasons: (i)The Schottcky barrier between the PS and its substrate for as prepared this junction have a large amount of dangling bond and surface channels [16], the oxidation start at the interface between the porous layer and silicon substrate where holes ,provided by the substrate are easily available to promote silicon oxidation subsequently making to the interface layer will be clean and decrease saturation current density subsequently decrease ideality factor [20]. (ii)because decreasing the density of state decrease after oxidation making to decrease ideality factor according to relation[20]:

$$n = 1 - \frac{\delta\varepsilon_s}{W\varepsilon_i} + \frac{\delta qD_s}{\varepsilon_i} \quad \ldots(10)$$

Where *Ds* in (cm^{-2} eV^{-1}) available to store charge in the inter phase layer at the semiconductor space charge region,*W* is the width of the semiconductor space charge region, ε_i, ε_s are the dielectric constant for the inter phase and semiconductor regions, respectively, where ε_i=3.9, and εs=11.9. Because increasing of the depletion layer width, also because increasing in oxide thickness (δ) which lead to increase the interface region thickness. Finally, we could observe that increasing of ideality factor with oxidation temperature larger than 600 that due to two reasons: (i)The initial of pin holes which play as a defect making to decrease detector efficiency [18]. (ii)The depletion layer width increasing with increase oxidation temperature lead to increase the ideality factor according to equation (9) .

For current transport across the barrier governed by thermonic emission and saturation current density given by the expression[16]:

$$J_S = A^{**}T^2 \exp\left(-q\Phi_{Bn}/KT\right) \quad \ldots(11)$$

Where A^{**} is the effective Richardson's constant, which equals 32($A/K^2.cm^2$) for P-type silicon and Φ_{Bn} (e V) is the barrier height while figure(5,b) shows the barrier height, it calculated from equation (10), the increasing in barrier height with increasing oxidation temperature was observed and it varied from (0-561to 0,698 eV). The increasing in barrier height with increasing oxidation temperature attributed to depending on the barrier height for PS on the barrier height of the M/PS/n-Si/M ,the PS/c-Si interface have pinning which acts as a defect in the interface and caused increase in saturation current [15], after oxidation the interface layer becomes clean by replacing unstable hydrogen and oxygen by pure and stable oxide atoms that decrease saturation current subsequently increasing barrier height[12-20] .

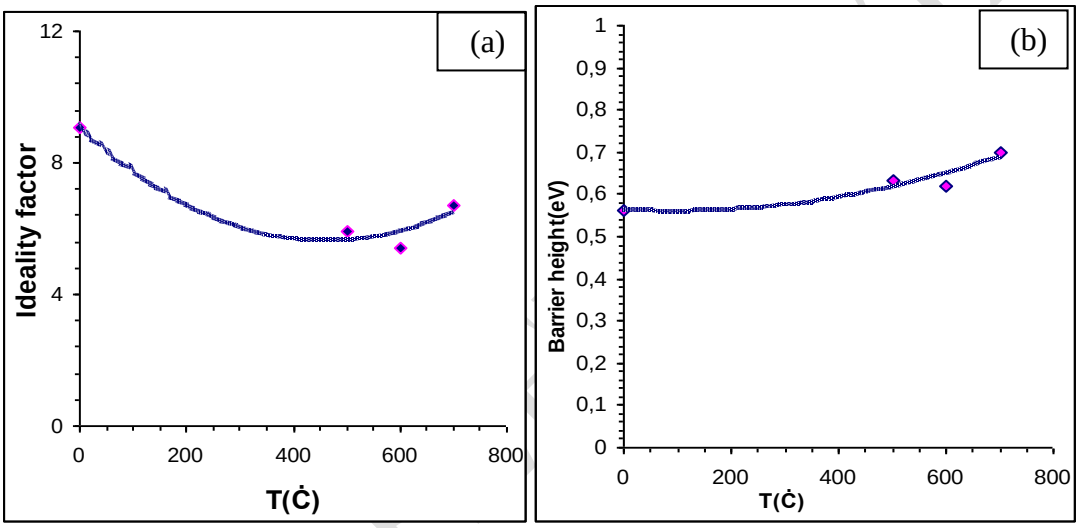

Figure 5. Shows(a) the ideality factor and (b) barrier height versus oxidation temperature.

4.Conclusions:

OPS/PS layer in this study formed by using rapid thermal oxidation process in atmosphere, The rapid thermal oxidation process didn't modify the morphology of porous layers. We only observed that the pore size decreased after oxidation . ,the pore density is conserved .Moreover ,the OPS layer was almost partially oxidized by the applied RTO oxidation process . The electrical properties under our optimum preparation conditions; the ideality factor, rectification ratio , and barrier height are measured at different oxidation temperature (500-700)Ċ ,the rectification ratio increased with increasing oxidation temperature from (3.93 to 158.8), ideality factor that describe approach device from ideality characteristics is founded decrease with increasing oxidation temperature where it varied from (9 to 5.4), the barrier height is increased from (0, 561 to 0,698 eV) that meaning the oxidation process working to consume column by growth within PS layer that changing Fermi-level and energy gap so decrease optical losses (backscattering, reflective notching ,and standing waves) that necessary for optoelectronic applications where the oxidation of PS layers is a good way to obtain lower optical loss of PS photo detector by reducing volume scattering and reflection also the oxide layer acts both as a protective and antireflection coating.

COMPETING INTERESTS DISCLAIMER:

I declared that no competing interests exist. The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts .

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