

Machine Capability Enhancement to Address Lacking Epoxy Coverage During Die Attach Process of QFN Packages

ABSTRACT

Epoxy coverage on die attach process is one of the important characteristics of a QFN semiconductor product. Epoxy condition on a die contributes to the product performance physically and electrically. Complete epoxy coverage satisfies the manufacturing requirement and resulting to customer's confidence. As the products becomes complex and innovative, certain difficulties are met on the production line. Incomplete epoxy coverage caused by epoxy hardening cannot be prevented as minor machine aid and other unscheduled machine idle time are present. This manuscript will discuss and focus on how to address the said phenomenon by automation principle and augmented process with the idea of industry 4.0.

Keywords: Die attach process; Integrated Circuits; epoxy position; QFN, automatic purge, dispenser, epoxy coverage, Design of Experiment

1. INTRODUCTION

Modernization has been one of the keys to successful manufacturing environment, providing high end quality products. With these qualities, end users and customers have proven their confidence and benefit to a solution where everyone benefits with suppliers and manufacturers. Application using modern technology such as internet of things, automation, robotics, and software upgrades are spent well to ensure continuous improvement from all aspects of processes are met.

Semiconductor manufacturing is one of the leading businesses in electronics industry. it includes IC's or Integrated Circuits that functions specifically design for a purpose. Almost everything we see inside and outside of our home shows different application of integrated circuits, from television, mobile phones, vacuum cleaners up to vehicles, traffic lights and billboards. While modernization of is continually evolving, this industry also goes with the current flow. Modern technologies are applied to produce high end commercial products and hybrid applications. One of the new products build by semiconductor companies is the Quad Flat No leads packages. Compared to conventional IC's this package does not use lead finger which is attached on an electronic board. Fig. 1. Shows a QFN package and an IC with lead fingers.

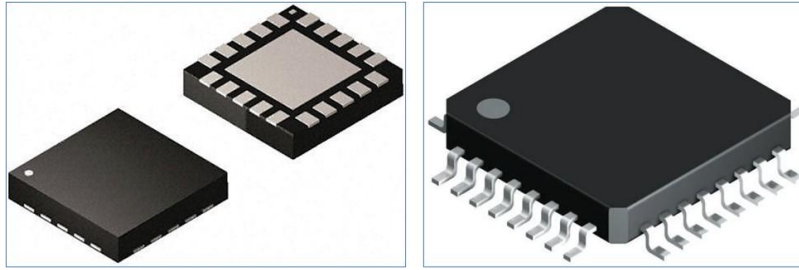


Fig. 1. Quad Flat No lead package (left) and conventional IC with leads (right)

Advantages of QFN's compared to other packages with leads are:

1. They are small, lightweight and occupies minimum space on the electronic board.
2. They are thin in construction and have a small form factor.
3. Interconnecting wires from frame to die are short.
4. They have good heat dissipation characteristic.
5. Low cost.

Process flow of QFN assembly starts in Front of Line or FOL stations with a material of silicon wafer that is singulated at a specific size and will be called as die. This die will be picked by die attach machine and will be attach on a leadframe using die attach material called epoxy. It will be cured in a certain temperature and will undergo die to leadframe interconnection called Wirebond process, wherein the die will be connected on the base leadframe by a thin wire made of gold. After these processes, next is the End of Line or EOL stations. The wire bonded units will be encapsulated by resin on molding process to cover the parts. After molding, leadframe will be singulated and marked as per customer's specification. Visual inspection and testing will be the final part of the assembly process.

Die attach as one of the critical processes on semiconductor manufacturing will be the focus of this manuscript. In this process of QFN packages, specific requirements are considered. Die attach criteria such as complete epoxy coverage are met to ensure that the design form, fit and function of the product is achieved. Epoxy coverage defined as the epoxy condition on all four sides of the die, and epoxy should be completely visible. **Desirable coverage output is projected though acceptable epoxy quality during dispensing.** As seen on Fig. 2. an example of epoxy pattern and complete epoxy coverage of the unit after die attach. Fig. 3. Shows an epoxy dispenser assembly of a die attach machine.

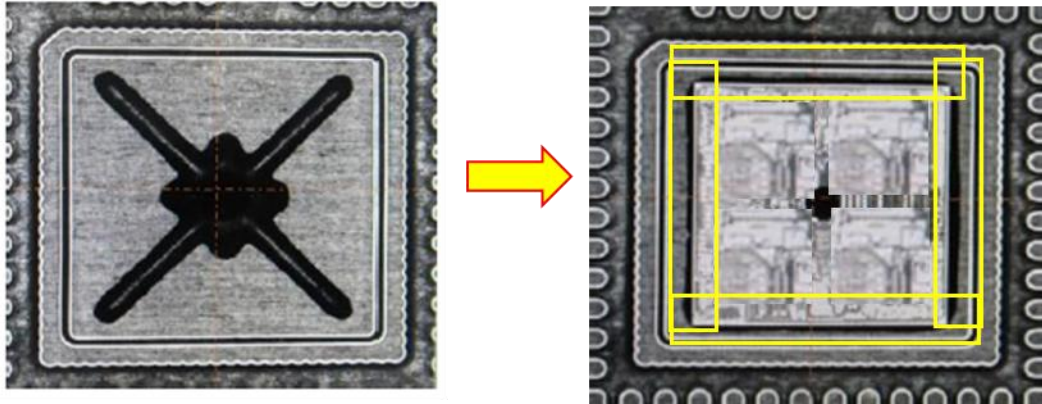


Fig. 2. Epoxy pattern dispensed on die pad, and Unit with complete epoxy coverage

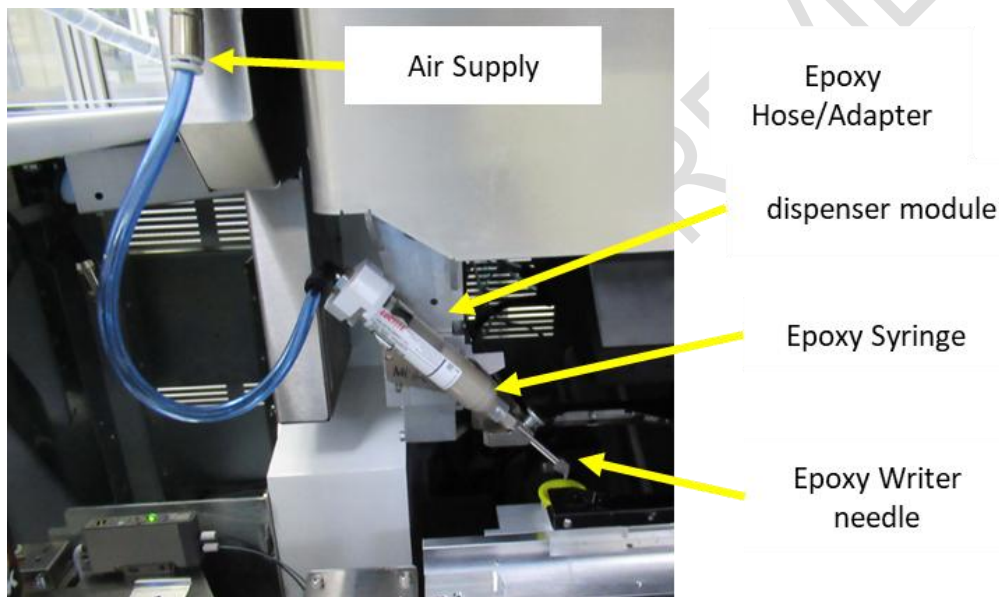
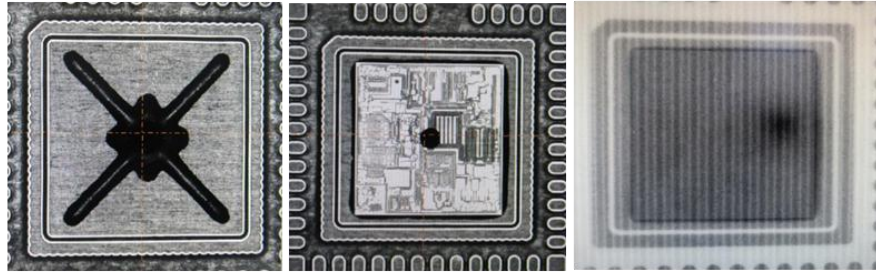


Fig. 3. Epoxy writer module of Die attach machine

Epoxy quality includes correct pattern ratio with respect to the die size, and completeness of the pattern. It also includes specific epoxy volume, epoxy pattern length and machine parameters defined by engineers. These factors affect the performance of every unit processed on the die attach machine. **Idle time is one of the contributors that affects the quality.** Die attach epoxy is known to hardened itself if not moving or flowing. This event is called idle time, meaning no movement of the epoxy due to some reasons like machine repair, absence of operator, or any machine assist during processing. Because of this event, epoxy tends to settle on the epoxy writer and causing to hardened itself. When this happens, clogging of the epoxy writer takes place during the initial dispense of epoxy. A clogged epoxy writer will reduce the volume amount of the dispensed epoxy resulting to incomplete epoxy pattern and incomplete epoxy coverage during die attach. Fig. 4. Shows a unit with insufficient epoxy coverage due to lacking epoxy volume. Four sides of the die area did not exhibit completeness of epoxy that may result to failed and defective units.

Ideal epoxy coverage on 4 sides of die



Insufficient epoxy coverage on 4 sides of die

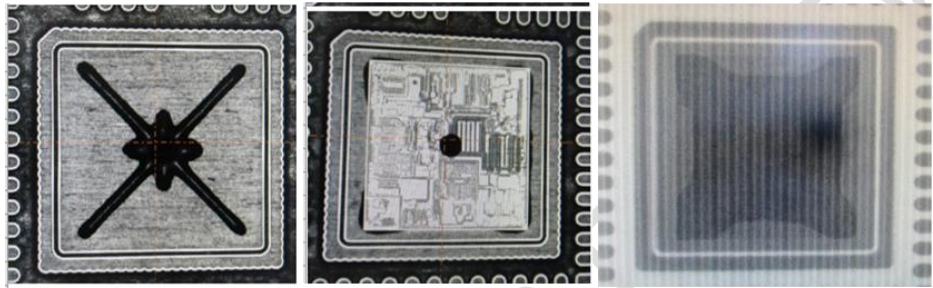


Fig. 4. Ideal and insufficient epoxy coverage shown on four sides of die

With this phenomenon, a robust and efficient action performed will be discussed on this manuscript. Simulations and statistical analysis are conducted to address the said defect and ensure the quality of the product.

2. METHODOLOGY

Given this assignable cause of the problem, a design of experiment is conducted to replicate the defect. This is to understand the occurrence on how it happened during the process, how long will be the allowable idle time to prevent, and how to address the occurrence of the defect.

The experiment consists of different idle time duration, to check the initial response of epoxy dispense pattern on the pad, and after die attach. Five runs were defined as seen on Fig. 5 and 6, categorized as:

- Run 1 – Time Zero (no idle time)
- Run 2 – 20 minutes idle time
- Run 3 – 30 minutes idle time
- Run 4 – 40 minutes idle time
- Run 5 – 60 minutes idle time

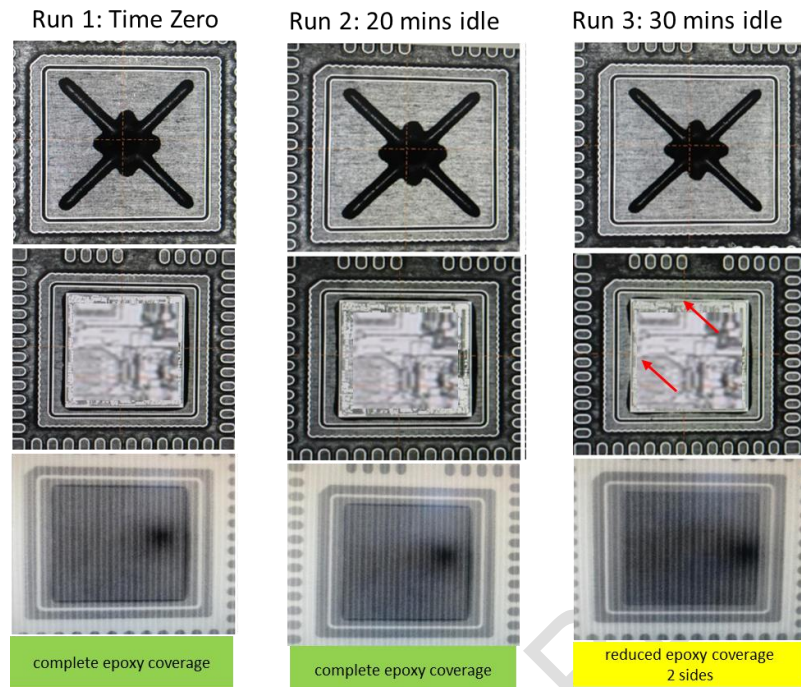


Fig. 5 Evaluation of idle time Runs 1-3

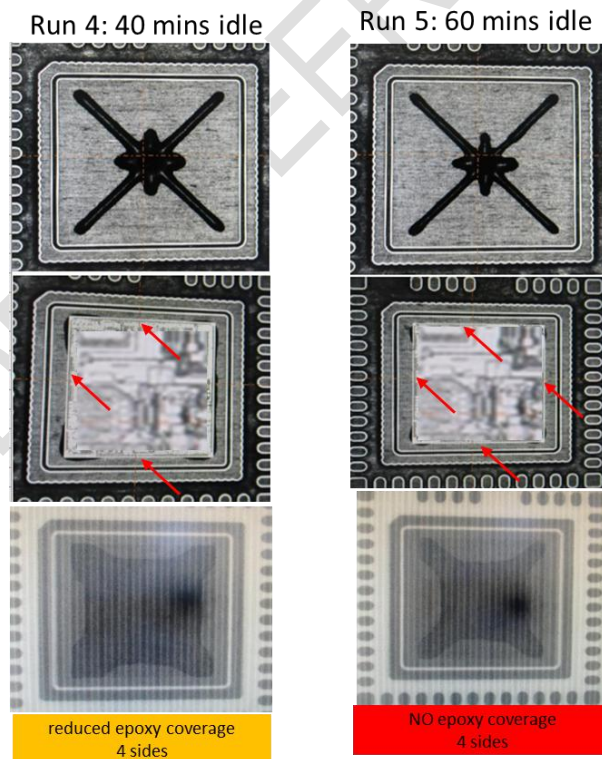


Fig. 6 (Cont.) Evaluation of idle time Runs 4-5

The first 3 runs show acceptable epoxy coverage on time zero, after idle time of 20 and 30 minutes respectively. Observed also on the images that epoxy patterns have been gradually reduced as idle time increases, resulting in lesser epoxy coverage on 2 sides of the die. Runs 4 and 5 with idle time of 40 and 60 minutes respectively shows worst result after die attach, not exhibiting epoxy coverage as seen on actual unit and X-ray images.

3. PROCESS IMPROVEMENT

Addressing the problem, idle time caused by unwanted reasons should be addressed by Modern machine feature to prevent clogging of the dispenser writer during process. This is to ensure that the initial dispense will still have enough epoxy volume to achieve complete epoxy coverage on units. The possibility of upgrading the machine feature comes to play. This is to introduce the dispense automatic purge and clean feature.

Automatic purge and nozzle clean feature from their words itself, is an upgraded feature of the machine wherein there will be a sequence of purging the epoxy prior start of the dispensing process after a specific idle time set on the machine. Same goes with the nozzle clean, wherein there will be a series of dispensing on a metal pad prior the dispensing process. Software and hardware is installed on the machine to complete the improvement package including the purging station consist of purging cup and cleaning place, and SW version update. Both of these features will remove the hardened epoxy caused by long idle time of the machine and prevent the occurrence of insufficient epoxy coverage on initial pads of the leadframe. As seen on Fig. 7 and 8 the purging station of automatic purge and nozzle cleaning, and its sequence upon activation:

1. START: Coming from Idle time, operator will continue the operation by pressing run.
2. POSITIONING: Dispenser will go to purging station, aligned to purging cup.
3. PURGE: Dispenser will purge epoxy at a specific time set on the parameters
 - a. (i.e. 4 seconds)
4. NOZZLE CLEAN: Dispenser will now go to cleaning plate and dispense a series of dot, to remove excess epoxy on the tip of the epoxy writer needle
5. PROCESSING: Dispenser will now start to process on good leadframes

There will be a specific time to be defined on the parameters, and upon reaching this time the sequence will take place.

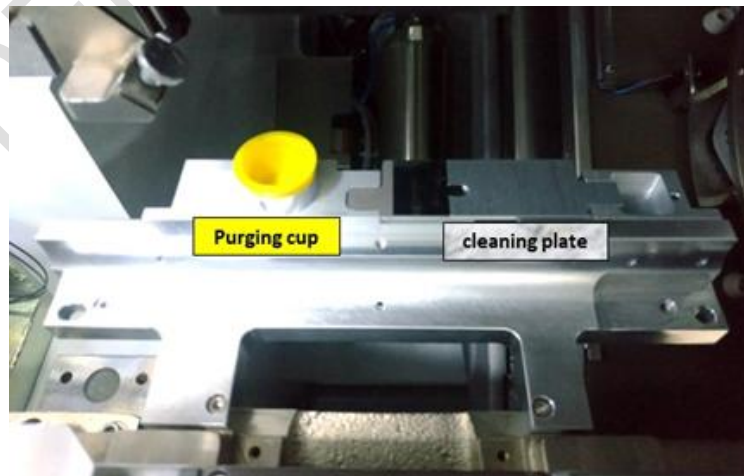


Fig. 7 Purging station installed for auto purge and nozzle clean feature

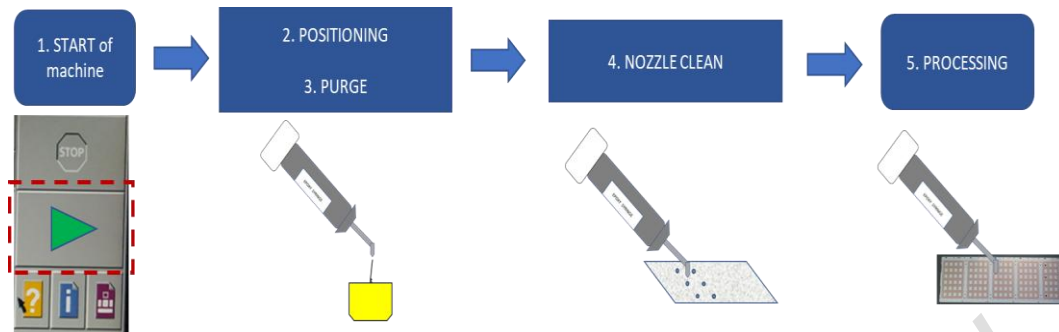


Fig. 8 Sequence of auto purge and nozzle cleaning

A second experiment is conducted to validate the effectivity of the improved machine capability of having automatic purge and nozzle cleaning. Evaluation will have 2 legs to be performed: First leg will have leadframe with 2 intervals of idle time during epoxy dispense, while the other leg will have the same interval but automatic purge and pre dispense is activated. See Figures. 9 and 10

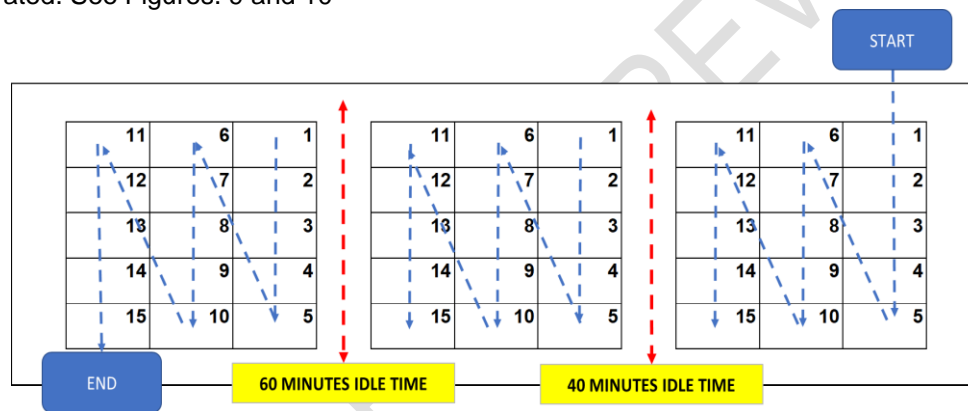


Fig. 9 die attach sequence of first leg, with 2 intervals of 40 and 60 minutes

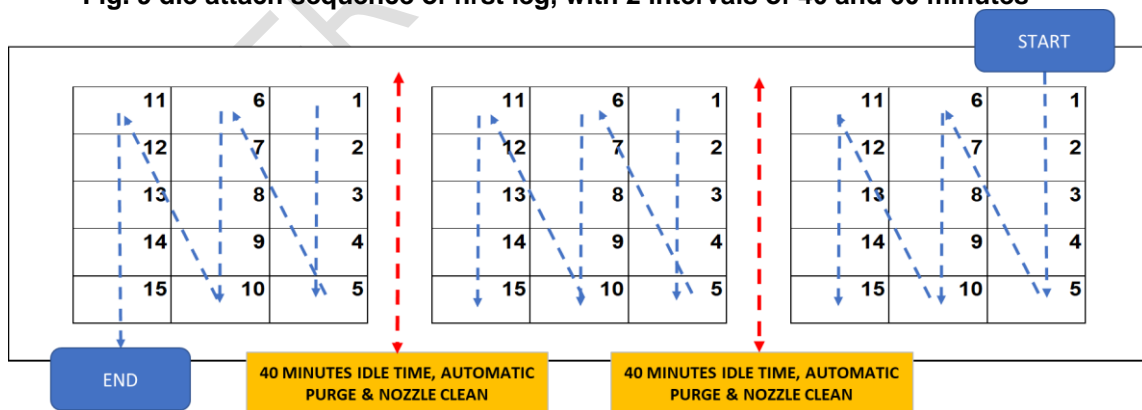


Fig. 10 die attach sequence of first leg, with 2 intervals of 40 and 60 minutes; automatic purge and pre dispense activated

3. RESULTS AND DISCUSSIONS

Based on the design of experiment performed to check the effect of idle time on the epoxy dispense, it has been observed that the longer the idle time occurs the lesser the epoxy volume will be dispensed initially on the die pad. Lesser epoxy volume will result to insufficient epoxy coverage that may affect product quality. This is projected on the first Design of Experiment and confirmed on this evaluation run with 40 and 60 minutes of idle time in between leadframe panels. With this idle time, several rejects of insufficient epoxy coverage have been recorded.

Compared to the first leg, the second with the automatic purge and nozzle cleaning shows significant difference and performance improvement, based on statistical analysis using chi square and 2-proportion tests. Mosaic plot show rejects on leg 1, while leg 2 projects all units have passed the epoxy coverage test.

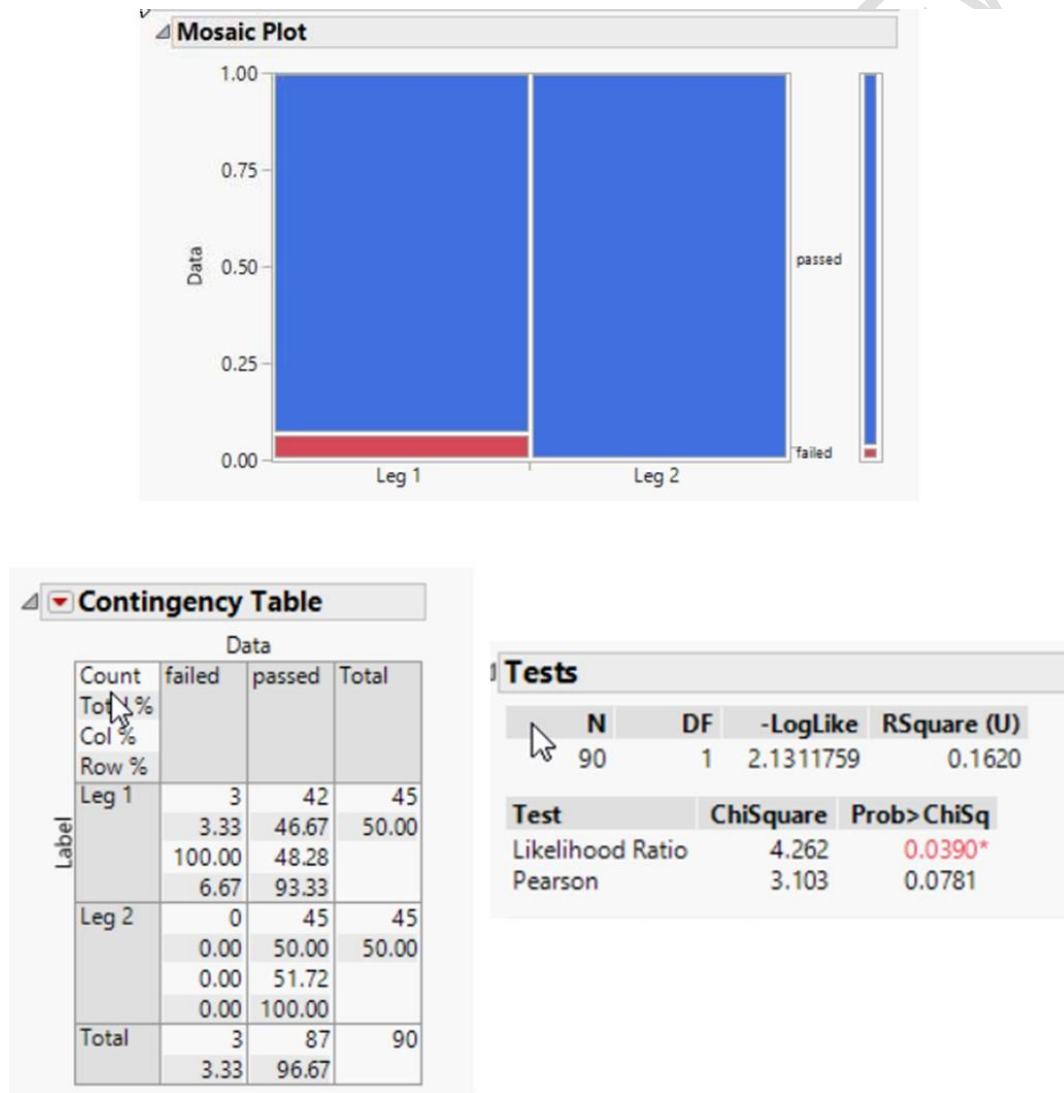


Fig. 11. Statistical analysis: Mosaic plot of Leg 1 vs Leg 2

3. CONCLUSION AND RECOMMENDATIONS

Having this automatic purge and nozzle cleaning features of die attach machine exhibit industrialized and automated improvement to have a robust die attach process. Preventing the chronic event of insufficient epoxy due to long idle time has been resolved by this breakthrough. Removing hardened epoxy on the epoxy writer needle was identified to be the rootcause, and introducing an automation makes the process more competitive to new and complex products of QFN packages. This has become an advantage for a more productive manufacturing and quality driven process. Applying the said innovation is recommended also on the same or equivalent process bricks and application of other products of semiconductor. References shared will be a benefit for experts to have inputs and learnings on the said topic.

REFERENCES

1. Eng TC, et al. Methods to achieve zero human error in semiconductors manufacturing. 2006 IEEE 8th Electronics Packaging Technology Conference (EPTC). Singapore. 2006;678-683.
2. Chan YK, et al. Image based automatic defect inspection of substrate, die attach and wire bond in IC package process. International Journal of Advances in Science, Engineering and Technology. vol. 6, issue 4, special issue 1, pp. 53-59, November 2018.
3. Abdullah Z, et al. Die attach capability on ultra thin wafer thickness for power semiconductor. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference. Malaysia: 2012;1-5.
4. Bacquian BC, et al. Bond line thickness characterization for QFN package robustness. Journal of Engineering Research and Reports. 2020;14(2);15-19.
5. Capili, M. D. (2020). Die Attach Pre-bond Inspection Innovation for Roughened Leadframe. Journal of Engineering Research and Reports, 16(1), 40-47. <https://doi.org/10.9734/jerr/2020/v16i117158>
6. Novin Yap, Caloy Hennosura, Freddie, Pascual, Elimination of epoxy bridging in diebond process. ON Semiconductor Philippines Inc
7. Raymond H. Meyers, Douglas C. Montgomery, Christine M. Anderson Cook. Response surface methodology: Process and product optimization using designed experiments 4 editions. Wiley; 2016.
8. Dinglasan, J. J., Saria, L. D., & Gomez, F. R. I. (2021). A Robust Approach of Maintaining Epoxy Position on Die Attach Process of Tapeless QFN Packages. Journal of Engineering Research and Reports, 20(6), 109-114. <https://doi.org/10.9734/jerr/2021/v20i617333>
9. Capili, M. D. (2021). Establishing Robust Control for Epoxy Open Time. Journal of Engineering Research and Reports, 20(3), 44-49. <https://doi.org/10.9734/jerr/2021/v20i317280>
10. L. C. Wai, D. M. Zhi, V. S. Rao and M. W. Daniel Rhee, "Process characterization of highly conductive silver paste die attach materials for thin die on QFN," *2012 IEEE 14th Electronics Packaging Technology Conference (EPTC)*, 2012, pp. 372-378, doi: 10.1109/EPTC.2012.6507110.
11. M. Arifin, N. Wivanius and N. F. Prebianto, "Epoxy Adhesive as Die Attach Material in Semiconductor Packaging: A Review," *2018 International Conference on Applied Engineering (ICAE)*, 2018, pp. 1-5, doi: 10.1109/INCAE.2018.8579410.

12. Chong D, Lim LY. Feasibility study on replacing conventional epoxy dispensing with wafer back coating epoxy for QFN packages for discrete product. In 2008 33rd IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT) 2008 Nov 4 (pp. 1-6). IEEE.
13. Hoe YY, Jie YG, Rao VS, Rhee MW. Modeling and characterization of the thermal performance of advanced packaging materials in the flip-chip BGA and QFN packages. In 2012 IEEE 14th Electronics Packaging Technology Conference (EPTC) 2012 Dec 5 (pp. 525-532). IEEE.

UNDER PEER REVIEW